[0089] An integrated circuit has a metal layer that includes conductors to provide interconnectivity for components of the integrated circuit chip. The metal layer is divided into at least two sections, such that a first section has a preferred direction and the second section has a preferred wiring direction that is different from the first preferred direction. The first and second preferred directions on a single metal layer may consist of any direction. The metal layer may be divided into more than two sections, wherein each section has a preferred wiring direction. Wiring geometries for multi-level metal layers are also disclosed

Figures

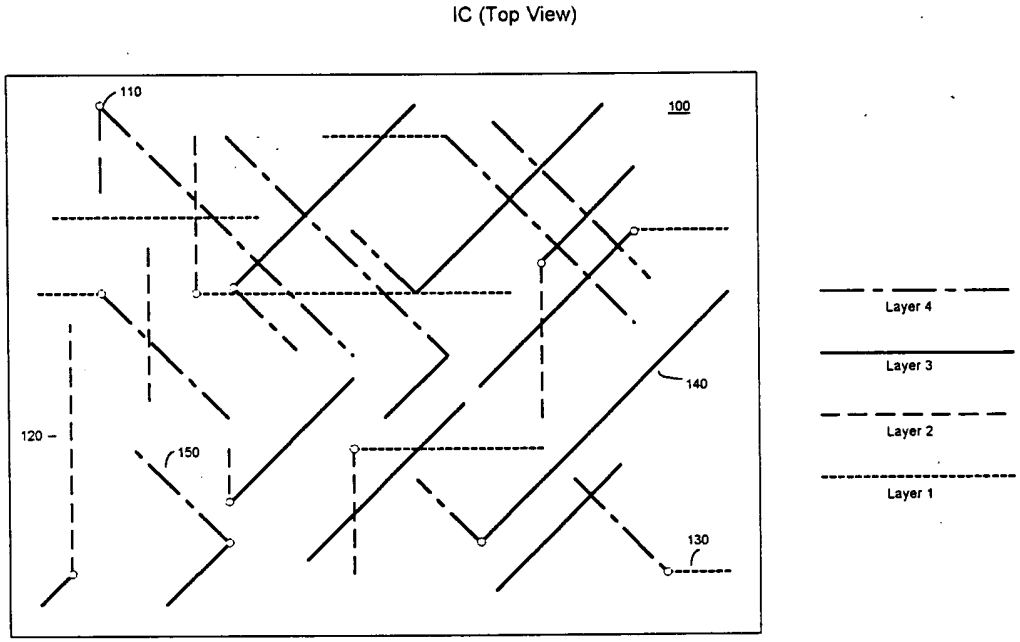


Figure 1a

IC (Top View)

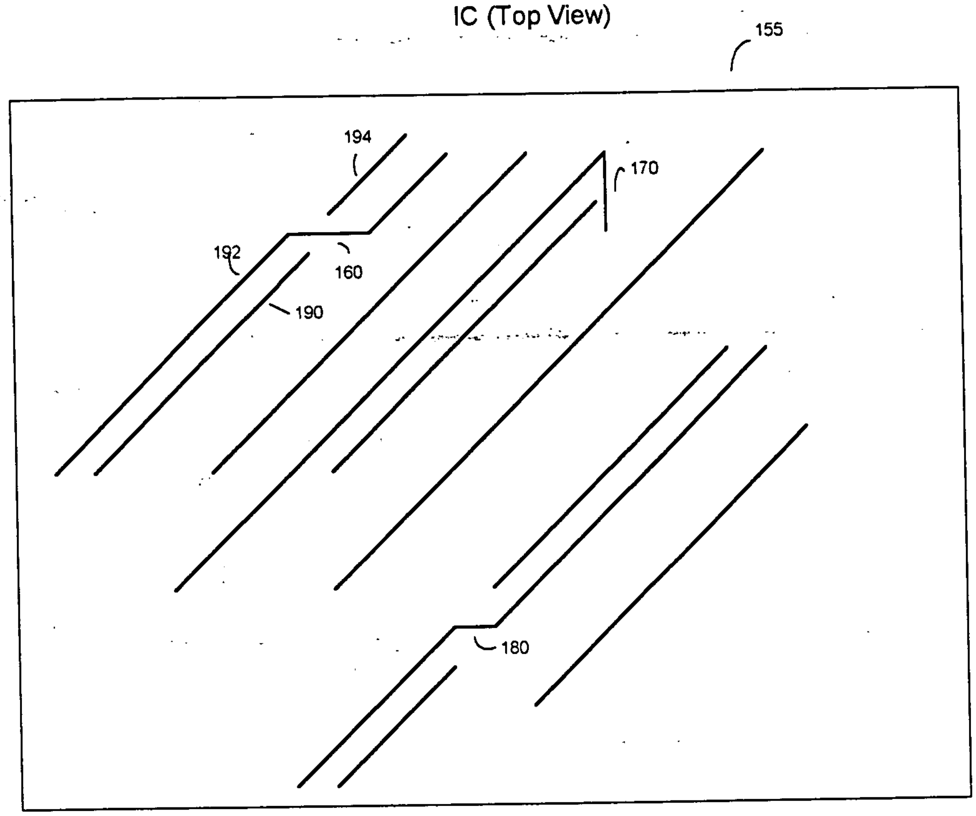
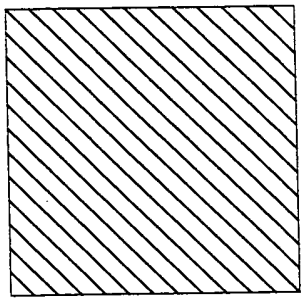
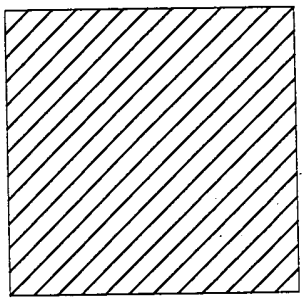


Figure 1b



Layer "n+1"

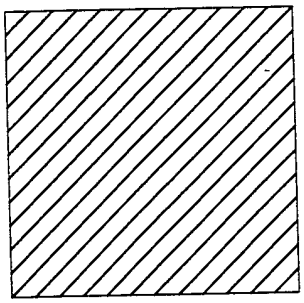
Octalinear (-45 Deg.)



Layer "n"

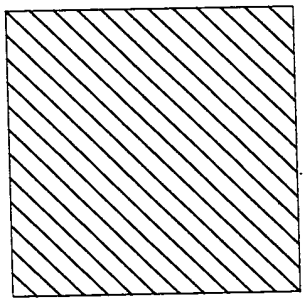
Octalinear (+45 Deg.)

Figure 2a



Layer "n+1"

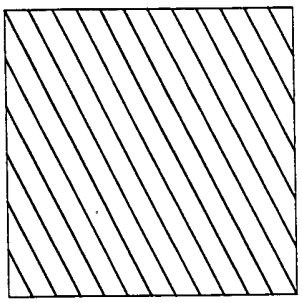
Octalinear (+45 Deg.)



Layer n

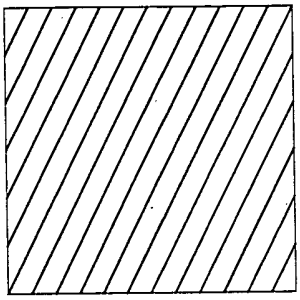
Octalinear (-45 Deg.)

Figure 2b



Layer "n+1"

(-60 Degrees)



Layer "n"

(+60 Degrees)

Figure 3a

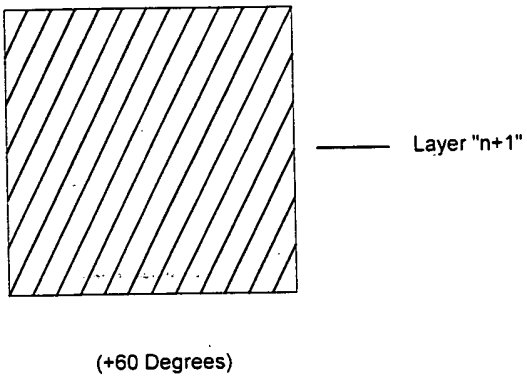


Figure 3b

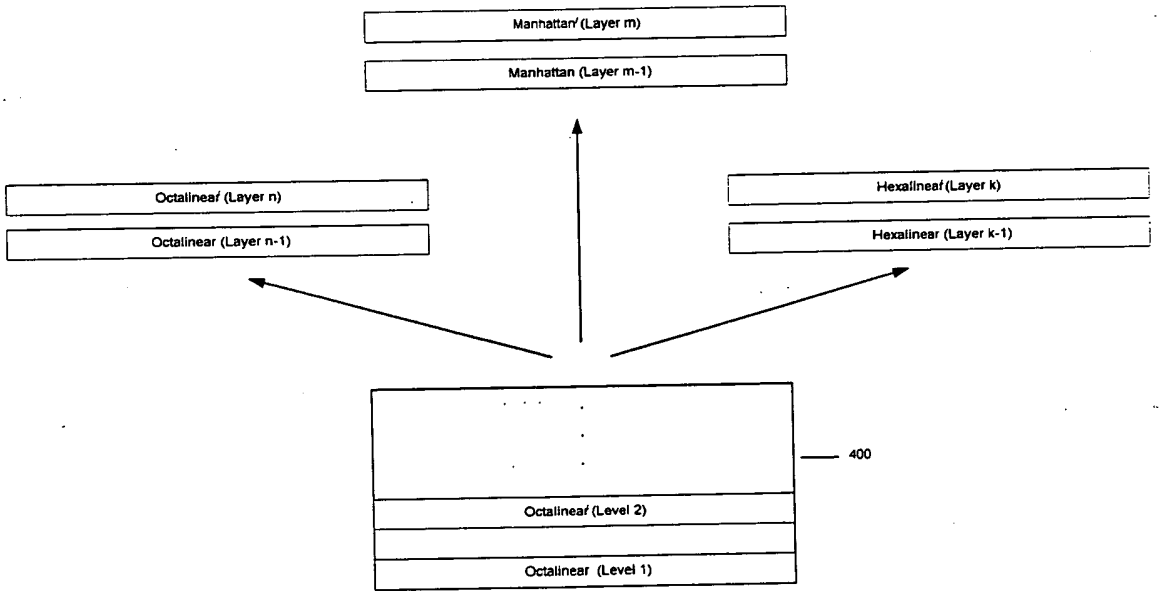


Figure 4a

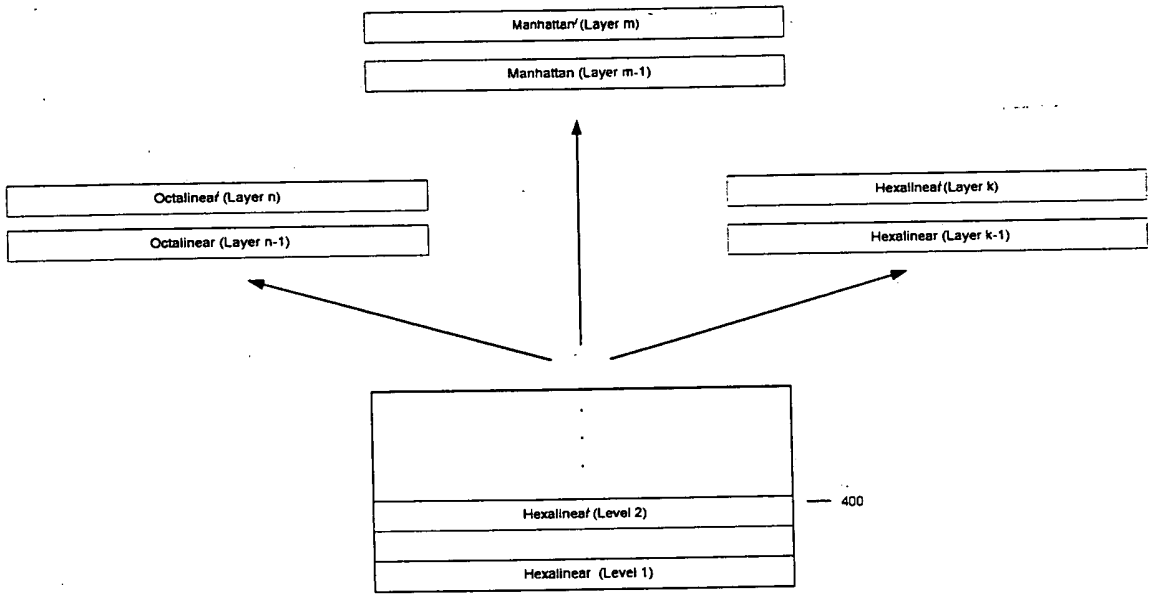


Figure 4b

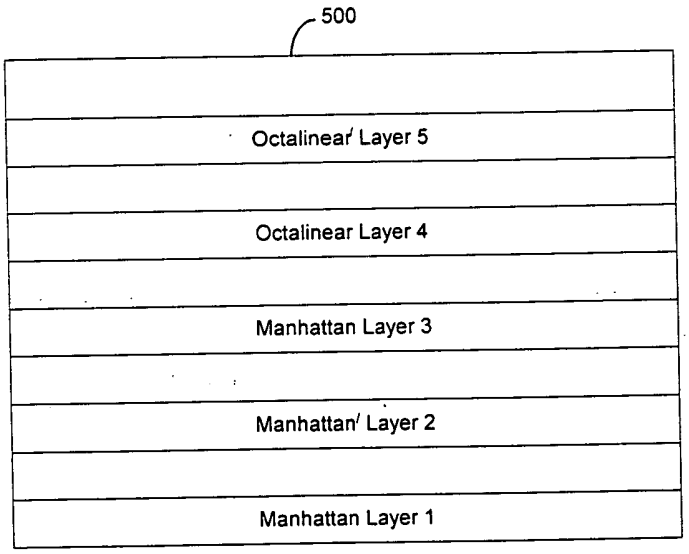


Figure 5a

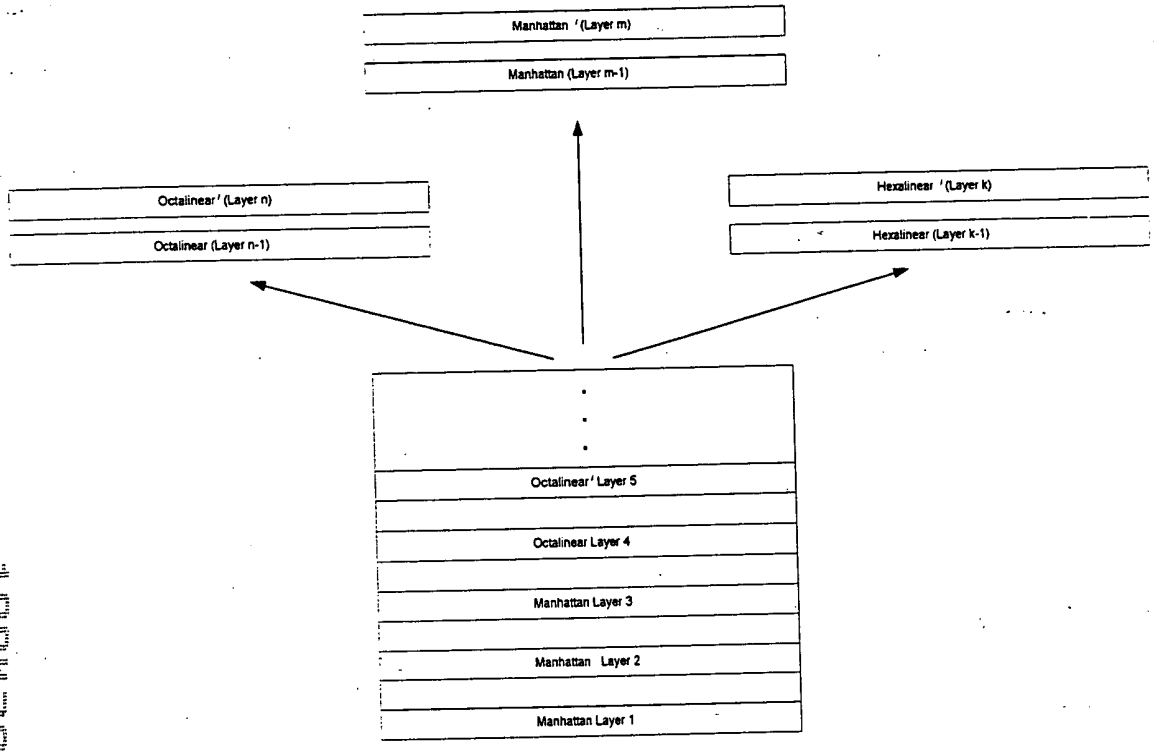
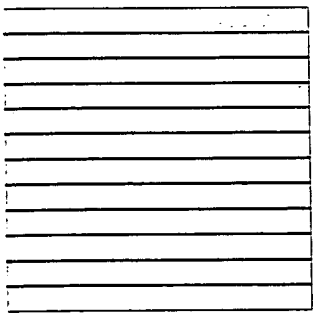
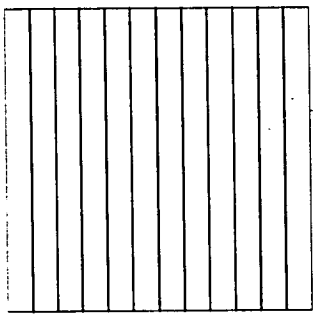

Manhattan ' (Layer m)
Manhattan (Layer m-1)
Octalinear ' (Layer n)
Octalinear (Layer n-1)
Hexalinear ' (Layer k)
Hexalinear (Layer k-1)
Octalinear ' Layer 5
Octalinear Layer 4
Manhattan Layer 3
Manhattan Layer 2
Manhattan Layer 1

Figure 5b



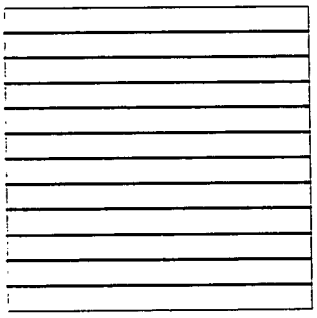
Layer 3

Horizontal



Layer 2

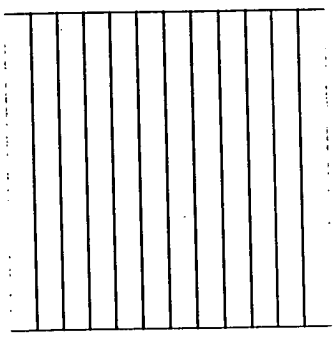
Vertical



Layer 1

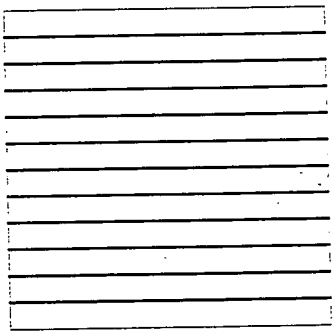
Horizontal

Figure 6a



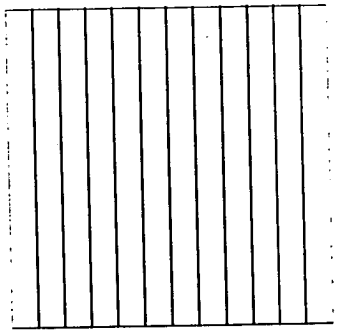
Layer 3

Vertical



Layer 2

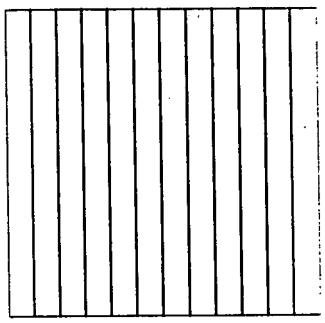
Horizontal



Layer 1

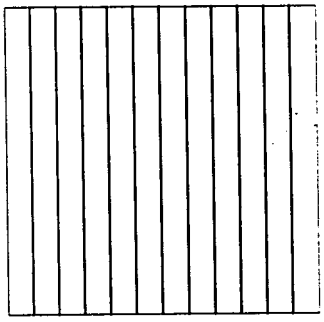
Vertical

Figure 6b



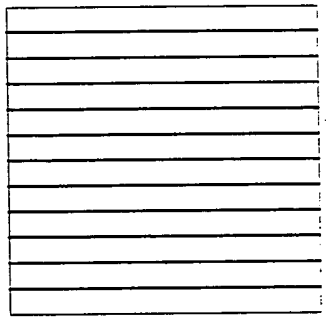
Layer 3

Vertical



Layer 2

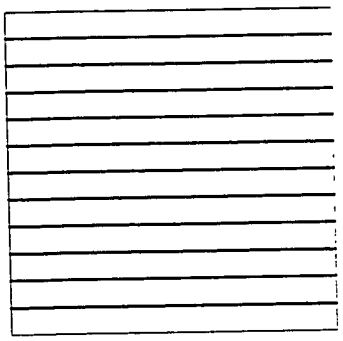
Vertical



Layer 1

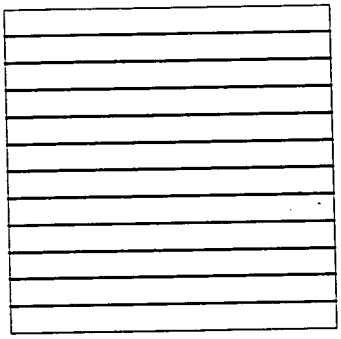
Horizontal

Figure 6c



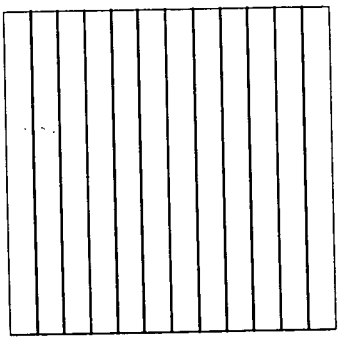
Layer 3

Horizontal



Layer 2

Horizontal



Layer 1

Vertical

Figure 6d

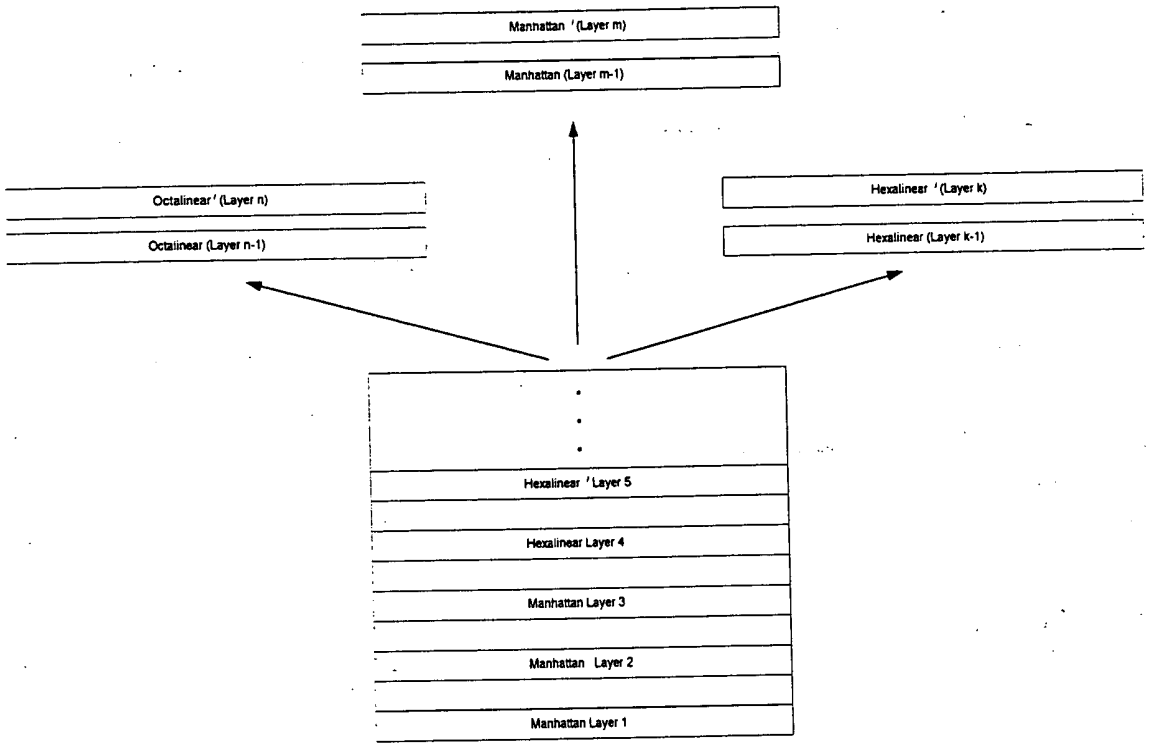

Manhattan ' (Layer m)
Manhattan (Layer m-1)
Octalinear ' (Layer n)
Octalinear (Layer n-1)
Hexalinear ' (Layer k)
Hexalinear (Layer k-1)
Hexalinear ' Layer 5
Hexalinear Layer 4
Manhattan Layer 3
Manhattan Layer 2
Manhattan Layer 1

Figure 7

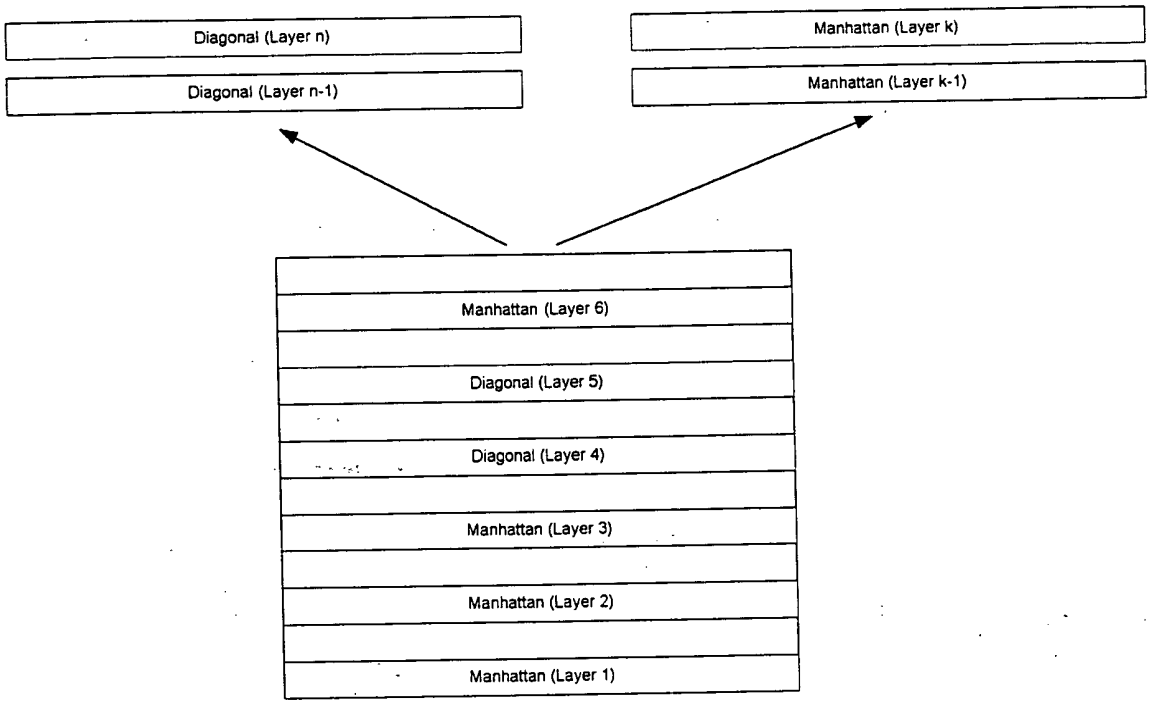

Diagonal (Layer n)
Diagonal (Layer n-1)
Manhattan (Layer k)
Manhattan (Layer k-1)
Manhattan (Layer 6)
Diagonal (Layer 5)
Diagonal (Layer 4)
Manhattan (Layer 3)
Manhattan (Layer 2)
Manhattan (Layer 1)

Figure 8

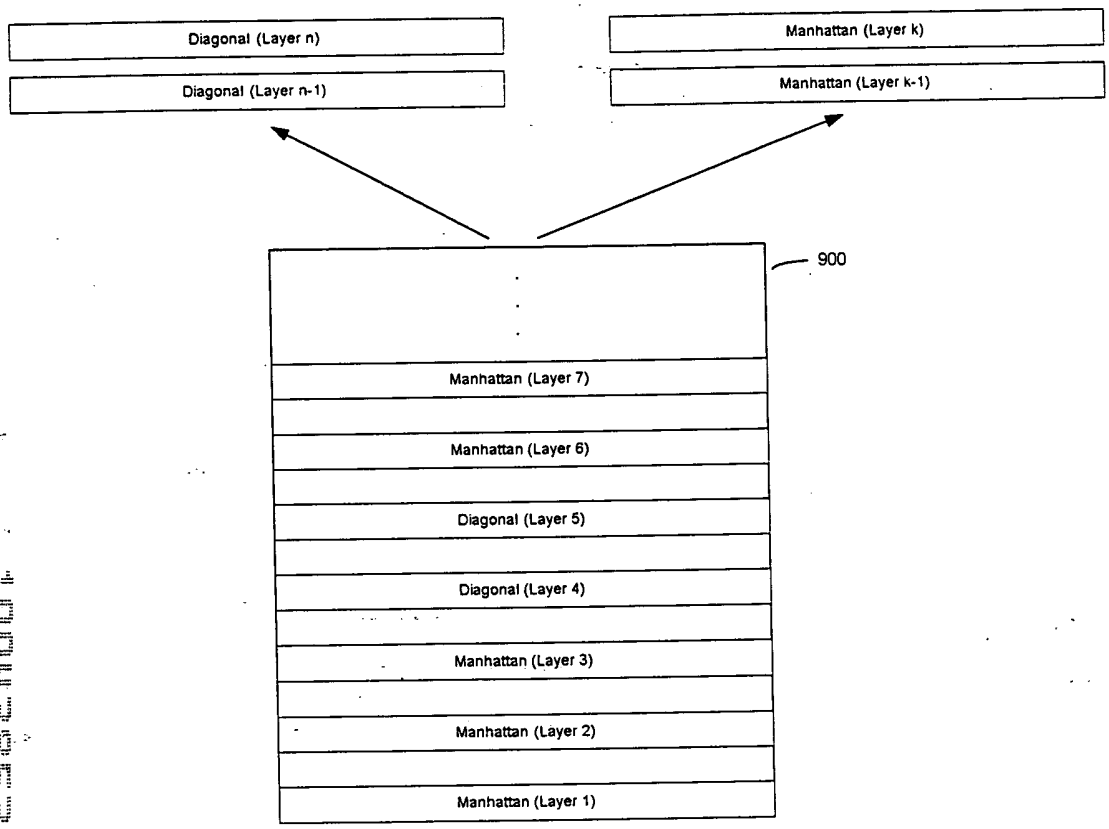


Figure 9

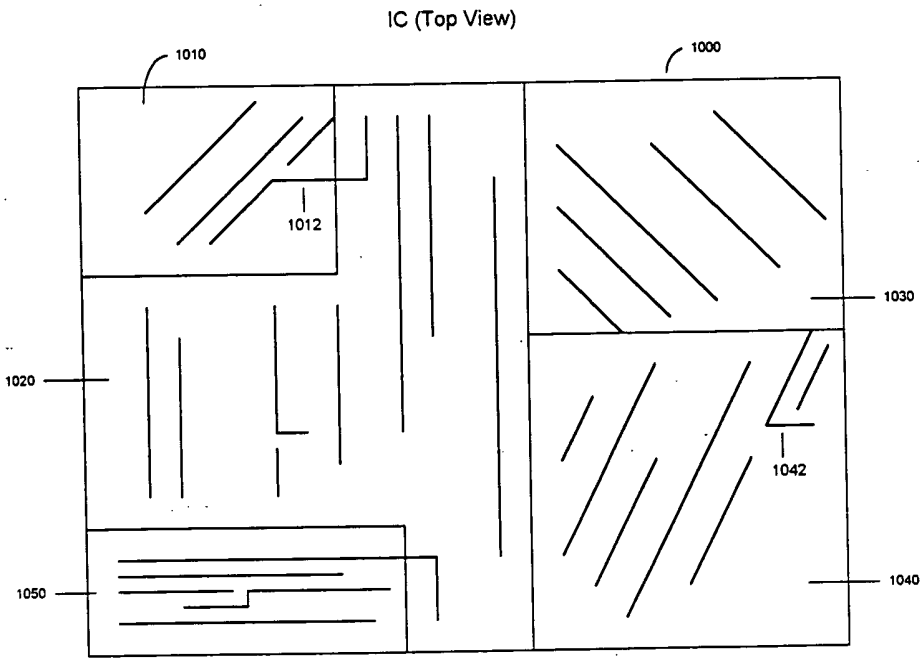


Figure 10

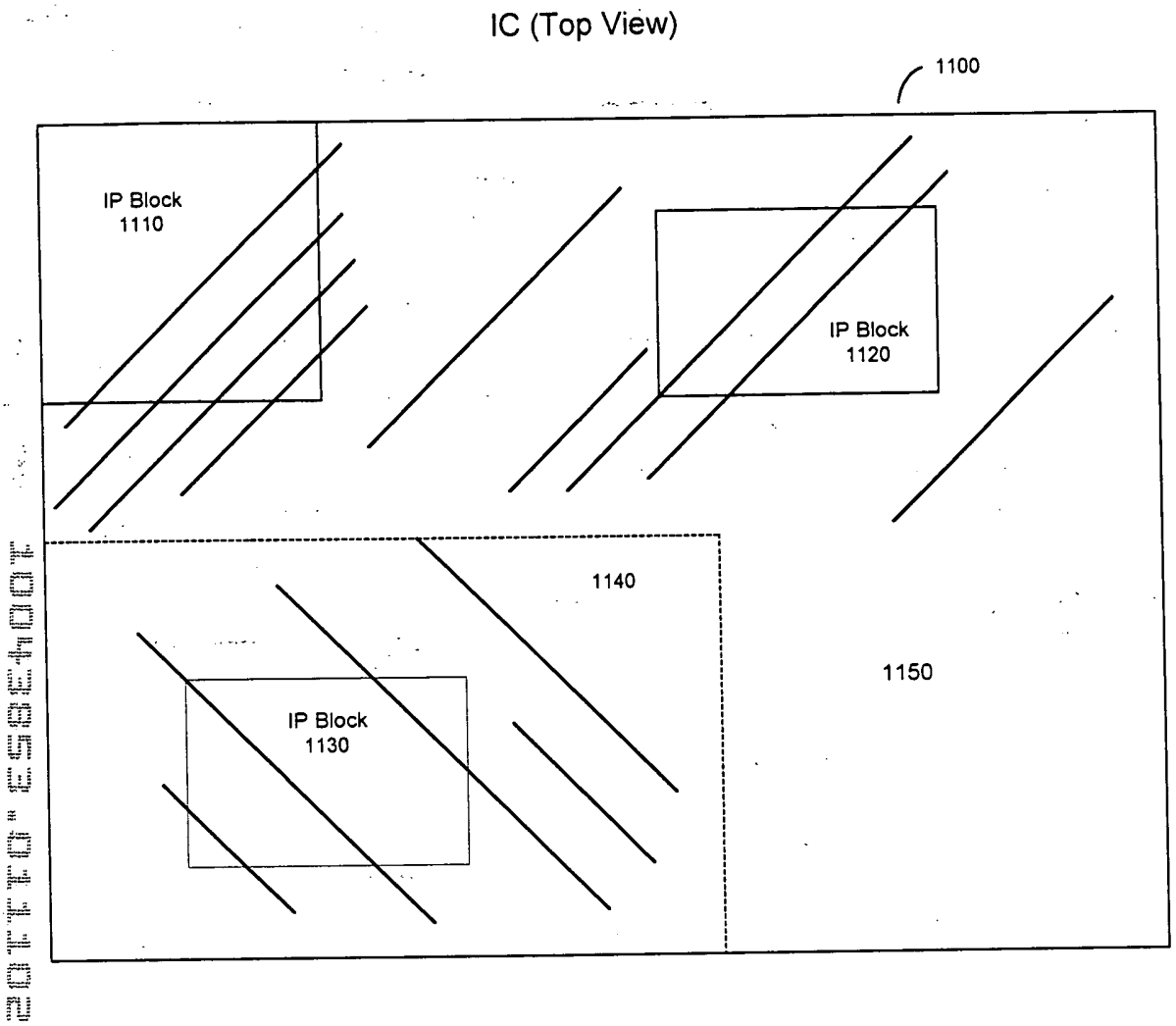

IC (Top View)
1100
IP Block
1110
IP Block
1120
1140
1150
IP Block
1130

Figure 11

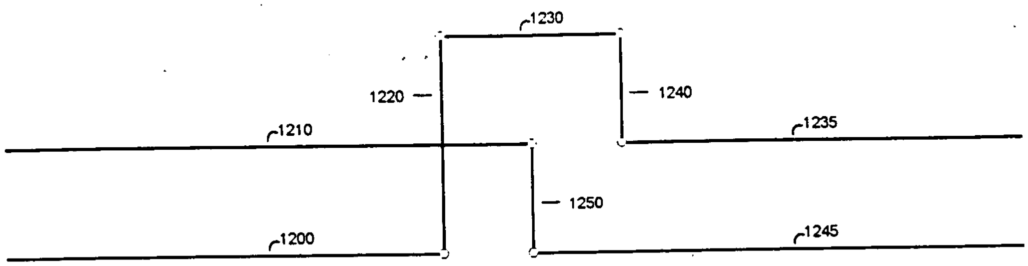


Figure 12a

Prior Art

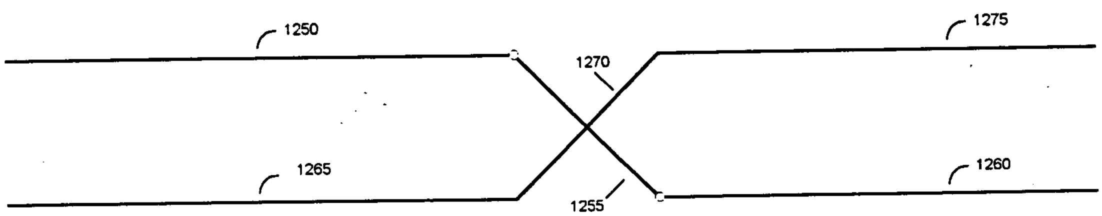


Figure 12b

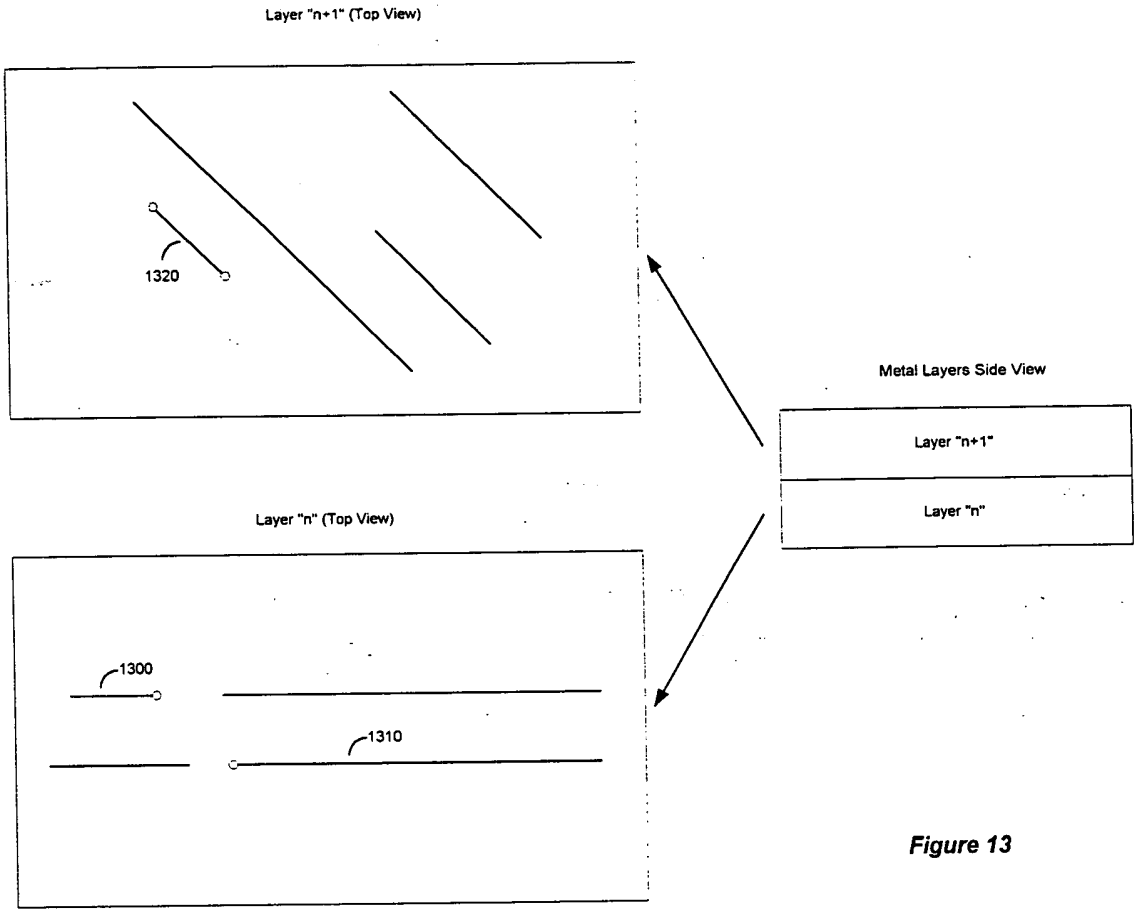

Layer "n+1" (Top View)
1320
Metal Layers Side View
Layer "n+1"
Layer "n"
Layer "n" (Top View)
1300
1310

Figure 13

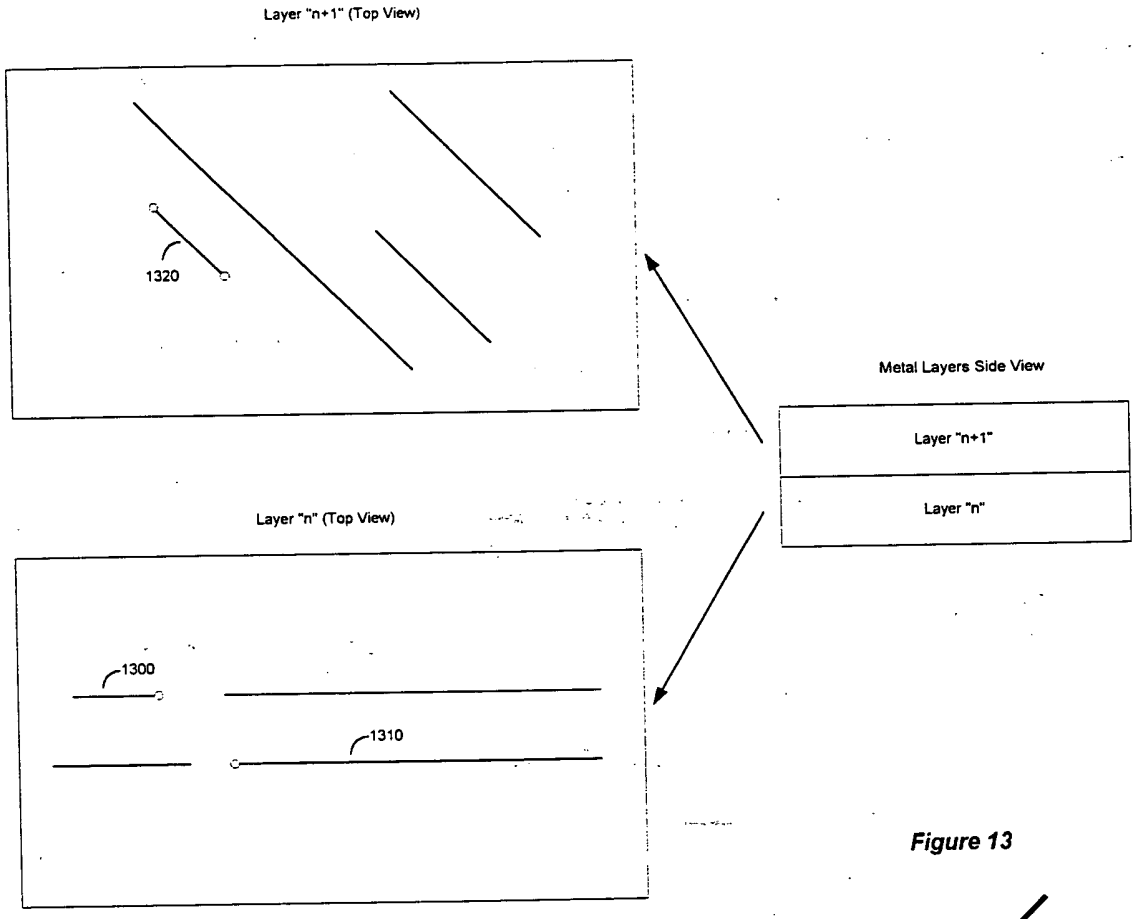


Figure 13

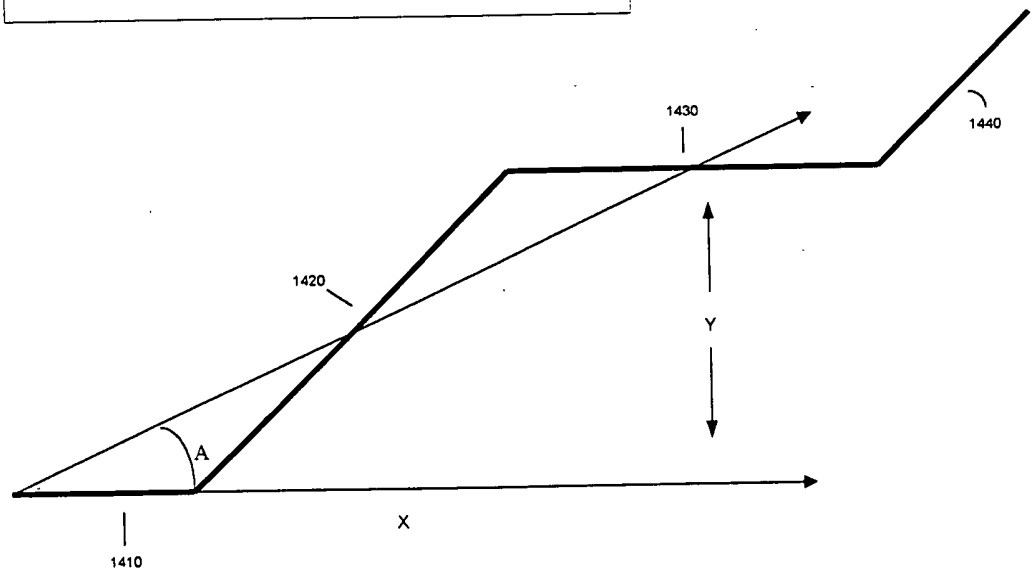


Figure 14

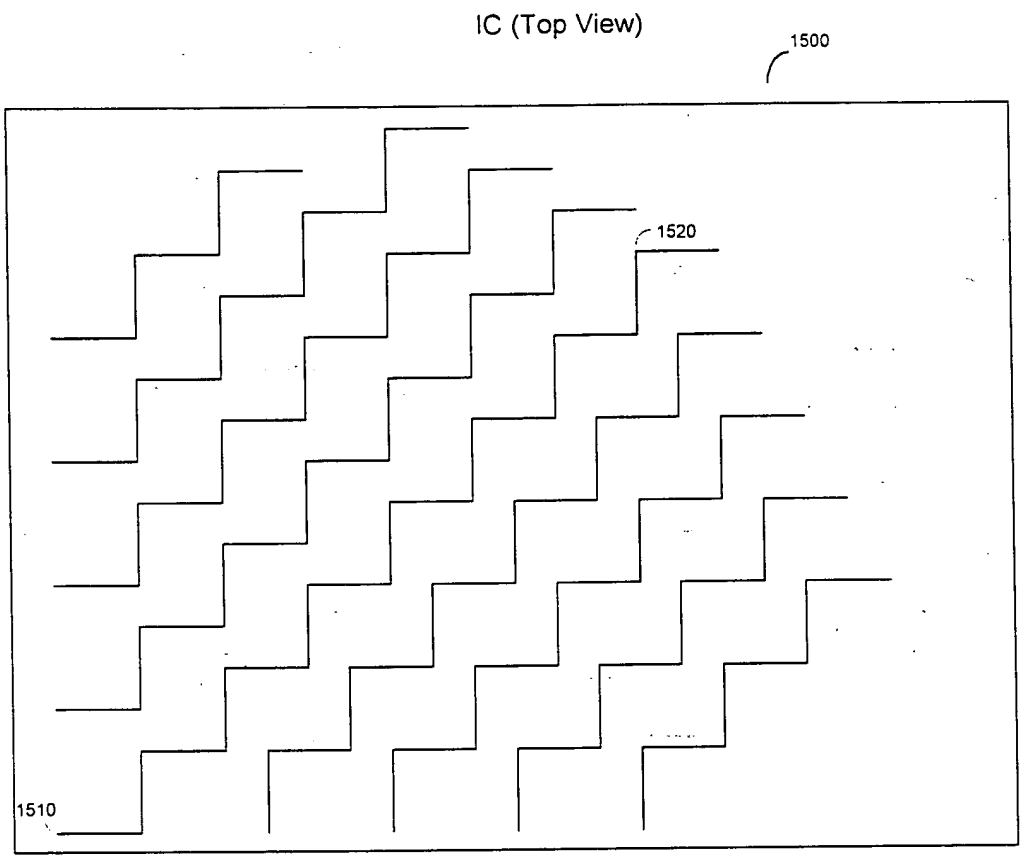


Figure 15

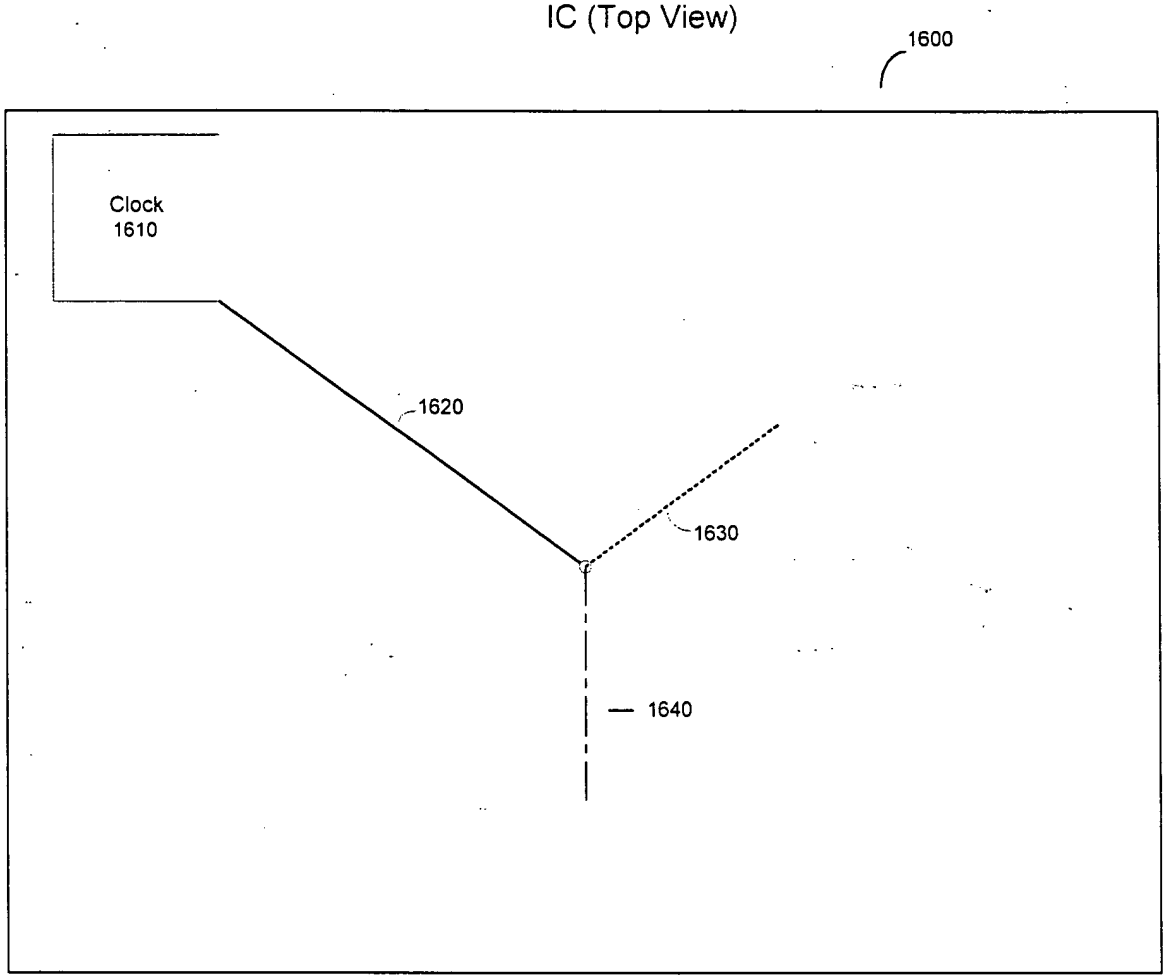


Figure 16